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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/830,068	04/23/2004	Young Joon Ahn	YHK-0135	7680

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EXAMINER	
DONG, DALEI	
ART UNIT	**PAPER NUMBER**
2879	

DATE MAILED: 10/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/830,068	AHN, YOUNG JOON	
	Examiner	Art Unit	
	Dalei Dong	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11-13 and 26-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-13 and 26-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The Amendment filed September 27, 2005, has been entered and acknowledged by the Examiner. The objection issued in office action on May 27, 2005, is withdrawn in light of the amendment filed on September 27, 2005.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3, 5, 11, 32 and 33 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,514,111 to Ebihara of record.

Regarding to claim 1, Ebihara discloses in Figures 1 and 2A-2C, a plasma display panel (1), comprising: a first substrate (22); a second substrate (27) facing the first substrate (22) with a discharge space therebetween; a sealing layer (32) located between the first substrate (22) and the second substrate (27); and a buffer layer (24a) formed between the first substrate (22) and the sealing layer (32) to compensate the thermal stress of the first substrate (22) and the sealing layer (32) (see column 5, lines 35-47); an upper dielectric layer (25) formed on the first substrate (2); and a protective film (26) formed on the upper dielectric layer (25) (see column 6, line 41 to column 7, line 6).

Regarding to claim 3, Ebihara discloses in Figures 1 and 2A-C, the buffer layer (24a) is formed by a low-melting-point glass paste mainly comprising lead oxide (see column 4, lines 27-38) and the first substrate (22) is made of glass which is a different material from that of the buffer layer and thus a range of thermal expansion coefficient of the buffer layer is different from a range of thermal expansion coefficient of the first substrate.

Regarding to claim 5, albeit, Ebihara discloses the buffer layer and the sealing layer both comprises mainly of PbO, however, Ebihara specifically discloses the buffer layer having a softening point of 580°C (see column 6, lines 41-53) and the sealing layer having a softening point of 400°C (see column 7, lines 37-48) and thus, the buffer layer and the sealing layer may comprises of the same material however with different component compositions. Therefore, a range of thermal expansion coefficient of the buffer layer is different from a range of thermal expansion coefficient of the sealing layer.

Regarding to claim 11, Ebihara discloses in Figures 1 and 2A-C, the upper dielectric layer (25) is formed on the buffer layer (24a) and the protective film (26) is formed on the upper dielectric layer (25) such that the buffer layer (24a) is provided between the first substrate (22) and the upper dielectric layer (25) and such that the upper dielectric layer (25) is provided between the buffer layer (24a) and the protective film (26).

Regarding to claim 32, Ebihara discloses in Figures 1 and 2A-C, a plasma display comprising: a first substrate (22); a second substrate (27) arranged with respect to the first substrate (22) such that a discharge space is provided therebetween; a sealing layer (32) between the first substrate (22) and the second substrate (27); a buffer layer (24a) provided on the first substrate (22) and provided between the first substrate (22) and the sealing layer (32) to compensate thermal stress of the first substrate (22) and the sealing layer (see column 5, lines 35-47); a dielectric layer (25) on the buffer layer (24a), the buffer layer (24a) being different than the dielectric layer (25); and a protective film (26) on the dielectric area such that the dielectric layer (25) is between the buffer layer (24a) and the protective film (26) and buffer layer (24a) is between the first substrate (22) and the dielectric layer (25).

Regarding to claim 33, Ebihara discloses in Figures 1 and 2A-C, the buffer layer (24a) is different than the upper dielectric layer (25).

4. Claims 26-28, 30 and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,495,262 to Igeta of record.

Regarding to claim 26, Igeta discloses in Figures 1-4, a plasma display panel, comprising: a first substrate (1B); a second substrate (1A) arranged with respect to the first substrate (1B) such that a discharge space is provided therebetween; a sealing layer (22a) between the first substrate (1B) and second substrate (1A); and a buffer layer (22b)

formed between the first substrate (1B) and the sealing layer (22a) such that the buffer layer (22b) is provided only in an area between the first substrate (1B) and the sealing layer (22a), the buffer layer (22b) to compensate thermal stress of the first substrate (1B) and the sealing layer (22a).

Regarding to claim 27, Igeta discloses in Figures 1-4, the sealing layer (22a) extends in a longitudinal direction (vertical direction) from a first end to a second end, the first end located proximal to the first substrate (1B) and the second end located proximal to the second substrate (1A), the buffer layer (22b) provided only in the area between the first end of the sealing layer (22a) and the first substrate (1B).

Regarding to claim 28, Igeta discloses in Figures 1-4, another sealing layer (22a on the opposite end thereof) between the first substrate (1B) and the second substrate (1A); and another buffer layer (22b on the opposite end thereof) formed between the first substrate (1B) and the another sealing layer (22a on the opposite end thereof) such that the another buffer layer (22b on the opposite end thereof) is provided only in another area between the first substrate (1B) and the another sealing layer (22a on the opposite end thereof), the another buffer layer (22b on the opposite end thereof) to compensate thermal stress of the first substrate (1B) and the another sealing layer (22a on the opposite end thereof).

Regarding to claim 30, Igeta discloses in Figures 1-4, a thermal expansion coefficient of the buffer layer (2B of 22b) is different from a thermal expansion coefficient of the first substrate (1B).

Regarding to claim 31, Igeta discloses in Figures 1-4, a thermal expansion coefficient of the buffer layer (2B of 22b) is different from a thermal expansion coefficient of the sealing layer (2A of 22a).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2 and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,514,111 to Ebihara of record in view of U.S. Patent No. 6,097,149 to Miyaji of record.

Regarding to claim 2, Ebihara discloses in Figures 1 and 2A-2C, a plasma display panel (1), comprising: a first substrate (22); a second substrate (27) facing the first substrate (22) with a discharge space therebetween; a sealing layer (32) located between the first substrate (22) and the second substrate (27); and a buffer layer (24a) formed

between the first substrate (22) and the sealing layer (32) to compensate the thermal stress of the first substrate (22) and the sealing layer (32) (see column 5, lines 35-47); an upper dielectric layer (25) formed on the first substrate (2); and a protective film (26) formed on the upper dielectric layer (25) (see column 6, line 41 to column 7, line 6).

Ebihara further discloses the buffer or dielectric layer (24) is formed by a low-melting-point glass paste mainly comprising PbO (see column 4, lines 27-38).

However, Ebihara does not specifically disclose the detailed composition of the dielectric layer as claimed.

The Miyaji reference teaches in Figures 1-5, a plasma display panel having a buffer layer (18) composed of PbO, B_2O_3, Al_2O_3 and SiO_2 (see column 7, lines 25-47) for the purpose of effectively forming a stable dielectric layer when different materials are used for forming bus electrodes in the plasma display panel.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have utilize the buffer layer of Miyaji for the plasma display panel of Ebihara in order to effectively form a stable dielectric layer when different materials are used to form the bus electrodes in the plasma display panel. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art.

Regarding to claim 7, the thermal expansion coefficient of the first substrate is merely a property of the material used in manufacture the first substrate, and the property

of the material does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations and thus this limitation has not given patentable weight.

Regarding to claim 8, the thermal expansion coefficient of the sealing layer is merely a property of the material used in manufacture the sealing layer, and the property of the material does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations and thus this limitation has not given patentable weight.

Regarding to claim 9, the thermal expansion coefficient of the buffer layer is merely a property of the material used in manufacture the buffer layer, and the property of the material does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations and thus this limitation has not given patentable weight.

6. Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,514,111 to Ebihara of record in view of U.S. Patent No. 6,495,262 to Igeta of record.

Regarding to claim 4, Ebihara discloses in Figures 1 and 2A-2C, a plasma display panel (1), comprising: a first substrate (22); a second substrate (27) facing the first

substrate (22) with a discharge space therebetween; a sealing layer (32) located between the first substrate (22) and the second substrate (27); and a buffer layer (24a) formed between the first substrate (22) and the sealing layer (32) to compensate the thermal stress of the first substrate (22) and the sealing layer (32) (see column 5, lines 35-47); an upper dielectric layer (25) formed on the first substrate (2); and a protective film (26) formed on the upper dielectric layer (25) (see column 6, line 41 to column 7, line 6).

However, Ebihara does not disclose the thermal expansion coefficient of the buffer layer is the same as the thermal expansion coefficient of the first substrate.

The Igeta reference teaches in Figures 1, a display panel, comprising: a buffer layer (2B) having thermal expansion coefficient same as thermal expansion coefficient of the first substrate (1B) (see column 8, line 60 to column 9, line 3) for the purpose of alleviating and absorbing the strain stresses between the first and second substrate during cooling and furthermore providing a hermetically sealed case which can stay stably airtight after it has been sealed off.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have utilize the buffer layer having same thermal expansion coefficient as of the first substrate of Igeta for the plasma display panel of Ebihara in order to alleviate and absorb the strain stressed between the first and second substrate during cooling and furthermore provide a hermetically sealed case which can stay stably airtight after it has been sealed off.

Regarding to claim 6, Igeta teaches in Figure 3, the thermal expansion coefficient of the buffer layer (22b) is the same as the thermal expansion coefficient of the sealing layer (22a) and the motivation to combine is the same as above.

7. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,514,111 to Ebihara of record in view of U.S. Patent No. 6,261,144 to Nishiki of record.

Regarding to claim 12, Ebihara discloses in Figures 1 and 2A-2C, a plasma display panel (1), comprising: a first substrate (22); a second substrate (27) facing the first substrate (22) with a discharge space therebetween; a sealing layer (32) located between the first substrate (22) and the second substrate (27); and a buffer layer (24a) formed between the first substrate (22) and the sealing layer (32) to compensate the thermal stress of the first substrate (22) and the sealing layer (32) (see column 5, lines 35-47); an upper dielectric layer (25) formed on the first substrate (2); and a protective film (26) formed on the upper dielectric layer (25) (see column 6, line 41 to column 7, line 6).

However, Ebihara does not disclose the buffer layer is formed to be extended from the upper dielectric layer.

The Nishiki reference teaches in Figure 7A, a plasma display panel having an upper dielectric layer (18) formed on the first substrate (14) and the buffer layer is formed to be extended from the upper dielectric layer (18) for the purpose of efficiently sealing of the plasma display panel.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have utilize the buffer layer extended from the upper dielectric layer of Nishiki for the plasma display panel of Ebihara in order to efficiently seal the plasma display panel.

Regarding to claim 13, Ebihara discloses the buffer layer (24) is separately formed of a different material from the upper dielectric layer (25) (see column 6, lines 34-65).

8. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,495,262 to Igeta of record in view of U.S. Patent No. 6,514,111 to Ebihara of record.

Regarding to claim 29, Igeta discloses in Figures 1-4, a plasma display panel, comprising: a first substrate (1B); a second substrate (1A) arranged with respect to the first substrate (1B) such that a discharge space is provided therebetween; a sealing layer (22a) between the first substrate (1B) and second substrate (1A); and a buffer layer (22b) formed between the first substrate (1B) and the sealing layer (22a) such that the buffer layer (22b) is provided only in an area between the first substrate (1B) and the sealing layer (22a), the buffer layer (22b) to compensate thermal stress of the first substrate (1B) and the sealing layer (22a).

However, Igeta does not specifically disclose the plasma display panel comprising an upper dielectric layer formed on the first substrate between the buffer layer and the another buffer layer; and a protective film formed on the upper dielectric layer.

Ebihara discloses in Figures 1 and 2A-C, an plasma display panel comprising: an upper dielectric layer (25) is formed on first substrate (22) between the buffer layer (24a) and the another buffer layer (32); and a protective film (26) is formed on the upper dielectric layer (25) for the purpose of reducing the stress in the dielectric layer of the sealing region, there by the occurrence of flaws therein is avoided without reducing the thickness of the dielectric layer in the display region.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have utilize the upper dielectric layer and a protective film of Ebihara for the plasma display panel of Igeta in ordér to reduce the stress in the dielectric layer of the sealing region, there by the occurrence of flaws therein is avoided without reducing the thickness of the dielectric layer in the display region.

Response to Arguments

9. Applicant's arguments filed September 27, 2005 have been fully considered but they are not persuasive.

In response to Applicant's argument that the prior art of record taken alone or in combination fails to teach or suggest buffer layer and upper dielectric layer. The Examiner asserts that Ebihara reference clearly teaches in Figures 1 and 2A-C, a buffer

layer (24a) and upper dielectric layer (25) in the plasma display panel. Thus, the Examiner asserts that the prior art of record teaches the claimed invention and maintains the rejection.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dalei Dong whose telephone number is (571)272-2370. The examiner can normally be reached on 8 A.M. to 5 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar Patel can be reached on (571)272-2457. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D.D.
October 19, 2005

Joseph Williams
Primary Examiner
Art Unit 2879